Fabrication and characterization of thermoelectric generators as *in situ* temperature sensor for III-nitride-based power transistors

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Abstract. The present work reports on the fabrication and characterization of a thermoelectric generator on the top surface of a power transistor in order to monitor its temperature indirectly through the thermo-generated voltage. The thermoelectric materials used for the generator were n-type Bi/Te and p-type Sb/Te deposited by co-evaporation process. We demonstrated for the first time the use of a thermoelectric generator to monitor the thermal health of III-nitride based power transistors.

Key words: *thermoelectric generator* (TEG), bismuth telluride, antimony telluride, Seebeck effect, temperature monitoring, temperature sensor, *high electron mobility transistor* (HEMT), *monolithic microwave integrated circuits* (MMICs).

1. Introduction

In recent years, III-nitride based *High Electron Mobility Transistors* (HEMTs) have become increasingly popular in the field of high power, high frequency and high temperature microwave systems. High power transistor reliability depends on the maximum operating junction temperature which can exceed 200°C. It is therefore necessary to develop ways to monitor in real time the junction temperature, in order to ensure reliability and device performance. A number of approaches have been used including that of an integrated *Surface Acoustic Wave* (SAW) sensor [1, 2].

Thermoelectric generators (TEGs) are used to convert heat into electricity (Seebeck effect). TEGs can become very attractive because they are compact,

require no moving parts and can be developed at relatively low cost. For temperatures up to 220^0C, *n*-type bismuth telluride (Bi_2Te_3) and *p*-type antimony telluride (Sb_2Te_3) thin films are the most efficient thermoelectric (TE) materials.

This work will report on the integration of a TEG on the top surface of an III-nitride based power HEMT in order to monitor its temperature indirectly through the thermo-generated voltage (HEMT-TEG).

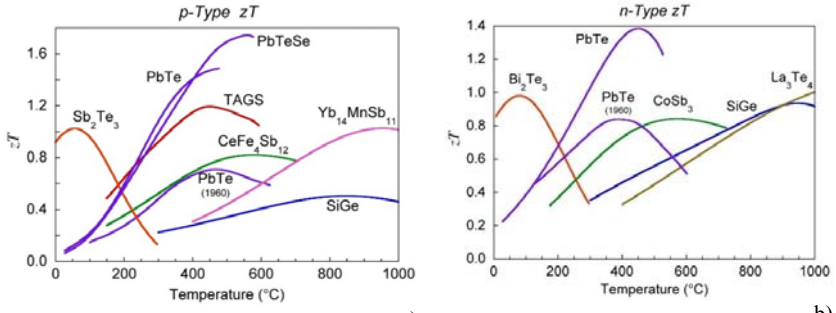
1. Experimental Procedure

In order to establish the correct technological platform for the HEMT-TEG concept, the study focused on three aspects:

1) Growing TE materials of optimum quality, like *n*-type Bi_2Te_3 and *p*-type Sb_2Te_3.
2) Developing optimized fabrication processing modules for the TEG, the HEMT and the HEMT-TEG.
3) Demonstrating for the 1st time the use of a TEG as temperature sensor monitoring the thermal health of III-nitride based power transistors.

Thermoelectric materials and optimization: TE materials can directly convert heat into electrical energy (Seebeck effect) and *vice versa* (Peltier effect). The efficiency of a TE device for electricity generation is given by the figure of merit (ZT) and expressed as $ZT=\frac{\sigma TS^2}{\lambda}$, where Sis the Seebeck coefficient, T is the temperature, σ is the electrical conductivity and λ is the thermal conductivity. To improve the efficiency (ZT), there is a need to simultaneously increase S and σ while reducing the thermal conductance. Since the variables are correlated to each other, increasing the ZT value greater than unity is a complicated task.

From a wide selection of TE materials, Bi_2Te_3 and Sb_2Te_3 compounds are considered good candidates for operation from room temperature up to 200°C. For *p*- and *n*-type materials, ZT values are in the range of 0.8 to 1.1 (Figure 1a and b respectively).



a) b)

Fig. 1. (Color on line). Figure of merit ZT of the most common used TE materials for thermoelectric power generation for (a) p-type and (b) n-type [3].

From published works [4, 5], the Seebeck coefficient and the figure of merit for *n*-type Bi_2Te_3 and *p*-type Sb_2Te_3 are listed below in Table 1.

Table 1. Seebeck coefficient and figure of merit for Bi_2Te_3 and Sb_2Te_3

Material	Seebeck coefficient (μV/K)	Substrate temperature (deposition) T_{sub} (^{0}C)	Electrical conductivity (Ohm*μm)	Figure of merit ($10^{-3}K^{-1}$)
Bi_2Te_3	− 248	270	12.6	2.87
Sb_2Te_3	188	220	12.6	1.63

The Seebeck coefficient of Bi_2Te_3 is negative and the Seebeck coefficient of Sb_2Te_3 is positive. If the two TE materials come into contact and combine to form a junction, then the Seebeck coefficient of the junction willbe.

$$S = S_{BizTea} - S_{SbzTea} = -\frac{436\mu V}{K}$$

In the present work, all depositions were carried out in a high vacuum chamber system (6×10^{-7} Torr), using co-evaporation thermal techniques. Each material evaporation was controlled by the respective "boat" current. In order to calibrate the co-evaporation process and optimize p- and n-type films, co-evaporations following overnight chamber pumping were performed, from high purity (99.999%) Bi, Te and Sb. The influence of the substrate temperature was also examined and optimized in the range between 25 and 150 ^{0}C. The deposition rates of both TE materials were controlled by a single crystal sensor. For the fabrication of Bi_2Te_3 films, the deposition rate of Bi and Te was calibrated between 0.1 − 0.2 nm/s and 0.3 − 0.8 nm/s respectively. A similar procedure was followed for the fabrication of Sb_2Te_3 films, the deposition rate of Sb and Te was calibrated between 0.1 − 0.2 nm/s and 0.3 − 0.8 nm/s respectively.

In order to optimize the deposition parameters and the influence of substrate temperature, the stoichiometric film composition and its structure were studied by *Energy-Dispersive X-ray spectroscopy* (EDX), *Field Emission Scanning Electron Microscope* (FE-SEM) and Hall measurements. In all cases, the Seebeck coefficients were measured at room temperature. One end of the TE material was connected to a heat sink, while the other end to a heater. The Seebeck coefficient of the TE material is a measure of the ratio of a potential difference (ΔV) across the material due to a temperature difference (ΔT). The temperature difference of the two ends is in the range of a few kelvin. The four point probe technique was used to measure the electrical resistivity. The *Power Factor* (PF) was determined using Equation 1, where $\rho$is the electrical resistivity (Ωm).

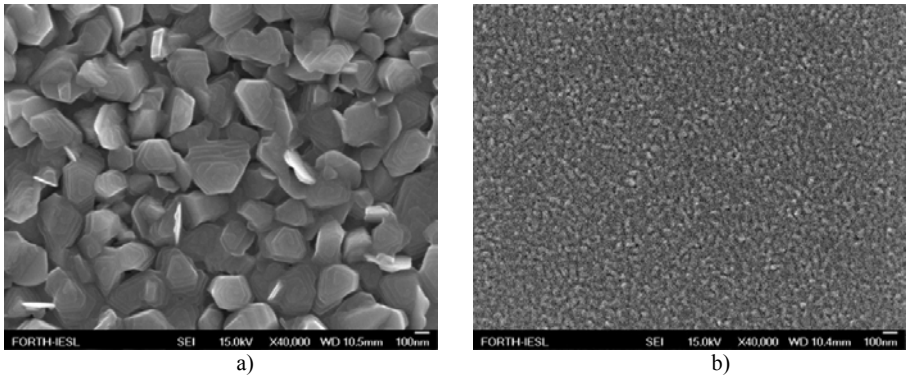
$$PF = S^2 / p \quad (1)$$

All the materials in this study were purchased from Test bourne Ltd. A series of Bi-Teand Sb-Te were fabricated at different flow ratio rates, stoichiometric compositions (at %) and substrate temperatures (T_{sub}) in order to optimize the TE material. Thermoelectric materials were deposited by co-evaporation and patterned by optical lithography using lift-off. Due to lithography, the presence of photoresist on the samples meant that the substrate temperatures during evaporation could not exceed 90^0 C which translates into not using the optimal substrate conditions for the thermoelectric materials growth. All TE films were 300nm thick (+10%). A study has been made of the thermoelectric properties of Bi_xTe_{1-x} and Sb_xTe_{1-x} films, and those that exhibit the best performance for T_{sub} up to 90^0 C are summarized in Table 2.

Table 2. TE properties of selected Bi_2Te_3 and Sb_2Te_3 films

Material	Stoichiometry	Temper. T_{sub} (^{0}C)	S(μV/K)	ρ(Ohm×m)	PF ($WK^{-2}m^{-1}$)
Bi : Te	1 : 2	85	− 52	8.5	0.32
Sb : Te	1 : 3	80	150	15	0.6

SEM images of the Bi-Teand Sb-Te samples were also taken as shown in Figure 2.



a) b)

Fig. 2. SEM images (a) Bi-Te and (b) Sb-Te surfaces.

The morphology of the samples was examined by FE-SEM. Both samples Bi-Te and Sb-Te were consisted of crystal grains, connected to each other. The Bi-Te exhibited grains with diameter up to 400 nm, while the Sb-Te showed much smoother surface with grains diameter up to 70 nm. The thickness of all samples was 300 nm.

HEMT-TEG. The basic processing steps used in fabricating the HEMT-TEG concept are divided into two sequential sub-processes. The first part has to do with

the fabrication of the power transistor (HEMT), while the second with the fabrication of the TEG on the top surface of the HEMT.

The fabrication of the HEMT was optimized on a 3 inch AlGaN/GaN epi-layers on Si substrate. After initial cleaning of the surface, the device fabrication started with the source and drain ohmic contacts, with a source-drain spacing of 5 μm. They were realized by the deposition of Ti/Al/Ni/Au (30/170/40/50 nm) combined with lift-off followed by *Rapid Thermal Annealing* (RTA) at 750 ^{0}C. Following, mesa isolation by reactive-on etching (RIE) in BCl_3/Cl_2 plasma etching was required for device electrical isolation. During this dry etching, part of the wafer was protected from the etchant by photoresist (masking material). After that, a Ni/Au (30/100 nm) gate, with a gate length of 1.5 μm, was formed between the source and the drain ohmic contacts again employing the lift-off approach. After the gate formation, a passivation layer of silicon nitride (Si_3N_4) was grown by *Plasma Enhanced Chemical Vapor Deposition* process (PECVD). The nitridelayer was approximately 200 nm thick and was deposited at 300 ^{0}C. Then a RIE step in SF_6 was performed to locally remove the Si_3N_4 layer. After Si_3N_4 etch, a deposition of Cr/Au (5/300 nm) metal layer and lift-off were used to connect all the gates and drains together with their pads contacts. Finally, the HEMT device was passivated with a second Si_3N_4 200 nm thick, deposited at 300 ^{0}C, in order to protect the top of the power transistor from environmental degradation and to "separate" the HEMT form the "TEG".

After finishing the fabrication of the HEMT, the TEG was fabricated on the top of the second Si_3N_4 passivation layer. N-type Bi_2Te_3 and *p*-type Sb_2Te_3 films 300 nm thick were deposited by thermal co-evaporation techniques. During evaporation the substrate temperature was in the range 85 – 95^{0}C and the working pressure was maintained below 6×10^{-7}Torr. The junctions between the *p* and *n* type layers were fabricated through the deposition of Nickel (Ni) 50 nm employing the lift-off process. The TEG device was finally passivated with a Si_3N_4 200 nm thick, deposited at 150 ^{0}C by PECVD. In order to access the contact pads of the HEMT-TEG, the Si_3N_4 was locally etched using RIE in SF_6.

All 11 photomasks used were designed using the "Clewin" software (Phoenix Technologies). Test structures have also been designed to enable the TE characterization. The detailed manufacturing process flow of the AlGaN/GaN HEMT-TEG and the information about the layers are shown in Figure 3. Phoenix Flow Designer simulates HEMT-TEG components and generates 2D pictures (cross sections).

Two approaches for the HEMT-TEG were designed. The one fabricates the TE modules on the top of the gate of the HEMT (Fig. 4a). Since we had concerns that the TEG could affect the RF performance of the power transistor, we also fabricated the TEG close to the gate (Fig. 4b).

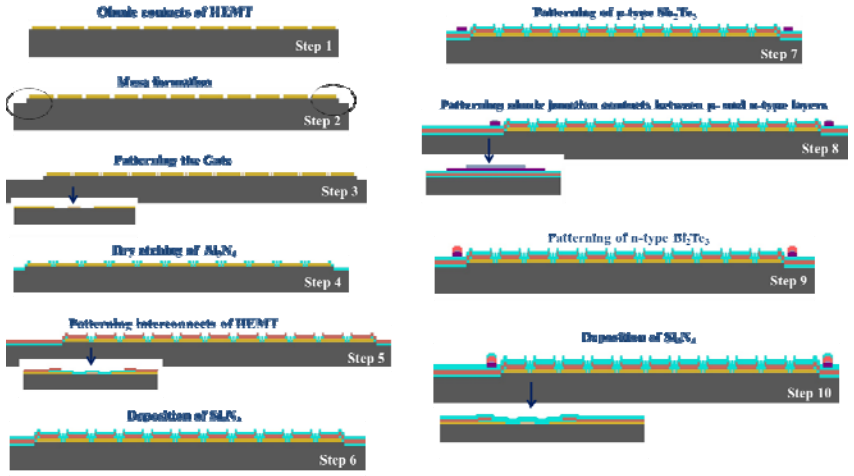


Fig 3. The fabrication process flow of a thermoelectric generator integrated on a AlGaN/GaN HEMT (simulations in Phoenix Flow Designer).

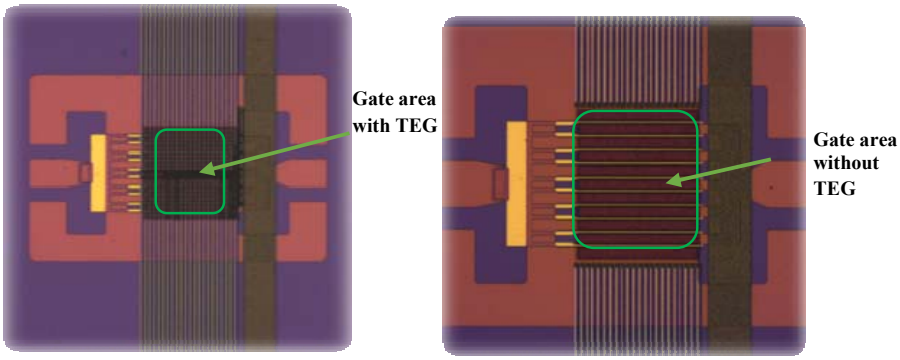


Fig. 4. (Color on line) HEMT-TEG device showing the thermoelectric modules (*p* and *n*-type) fabricated (a) on top of the gate HEMT structure and (b) closed to the gate HEMT structure.

3. Results and Discussion

HEMT-TEG DC & RF characterization: The characterization was performed using a RF probe station connected toa Keithley 2604B and HP8510B

VNA. Initially the transistor was characterized in relation to its DC and RF performance prior to the TEG fabrication. The same set of tests were performed on the transistors after the realization of the TEG. As expected we noticed no difference in the DC performance of the devices.

Figure 5 shows the typical DC behavior of a transistor for different gate voltages. The source-drain current was limited by the VNA current restriction,

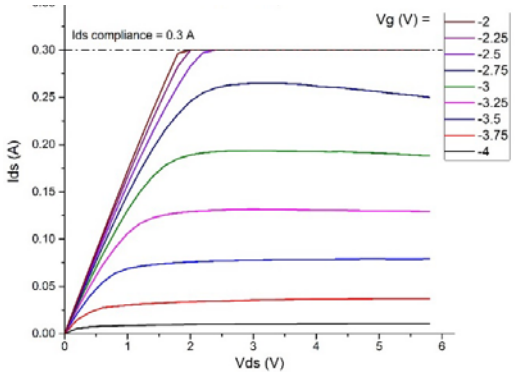


Fig. 5. (Color on line). Typical behavior of the drain current (I_{ds}) as a function of drain voltages (V_{ds}) for different gate voltages (V_g).

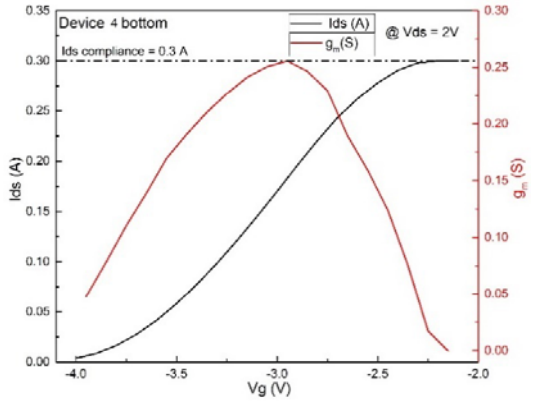


Fig.6. Source-drain current I_{ds} (left axis) and Transconductance (g_m) non normalized to the gate width (right axis) as a function of V_g at constant V_{ds} = 2 V.

which is 0.3 ampere. The power transistor shows a good saturation and pinch-off characteristics. Sweep of the gate voltage at the constant source-drain voltage (Fig. 6) allows us to calculate a transconductance (g_m) from the slope of I_{sd} *vs* V_g, following the formula: $g_m = dI_{ds}/dV_g$

The presence of TEG layers on top of the HEMT (Fig.8) could lead to spurious capacitances that could appear during the RF performance of the device. To clarify this issue we performed RF characterization before and after the fabrication of the TEG. The maximum available power gain (G_{max}) as a function of frequency was obtained form S-parameter measurement at V_{DS}=6V (Fig. 7).

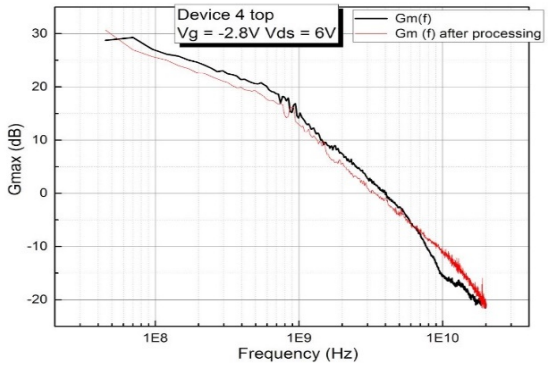


Fig. 7. Maximum available gain (G_{max}) as a function of frequency. The fabrication of TEG layers did not affect the RF behavior of the transistor.

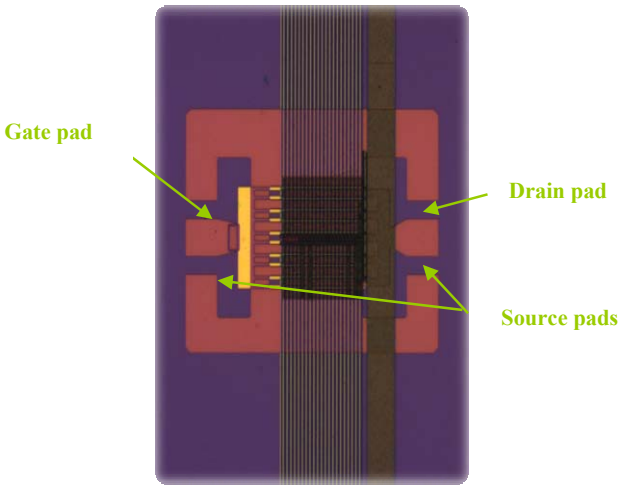


Fig. 8. Finalized HEMT –TEG.

AlGaN/GaN ***HEMT-TEG performance.*** The evaluation of the thermoelectric

generator as *in situ* temperature sensor was performed at room temperature using a Keithley 4200-SCS/F semiconductor characterization system analyzer. The flow of current in the power transistor produces heat at the junctions at the gate regions. Any increase in current flow through the transistor will result in transistor heat up. For AlGaN/GaN HEMTs a typical maximum junction temperature is up to 220^0C (NITRONEX Corp. [6]).The TEG must be triggered by the heat from the transistor and in this way we can monitor the temperature indirectly through the thermo-generated voltage. Several experiments were conducted to measure the thermal voltage of the TEG. The DC I-V measurements employed a drain-source voltage V_{DS} = 0 V to 9 V and a gate-source voltage V_{GS} = 0V. The experimentally measured thermo-generated voltage curves (colored lines) across the TEG as a function of operating time of the transistor, for different drain-source voltages, are presented in Figure 9. The total Seebeck is expressed as

$$S_{total} = S_{BizTea} - S_{SbzTea} \approx -\frac{202\mu V}{^0C} \tag{2}$$

Therefore, the generated thermo-voltage across the TEG (micro generator consists of N = 22 thermocouples) is

$$V_{th} = \left|S_{total}\right| xN\left(thermoelectricpairs\right) \approx \frac{3.5mV}{^0C} \tag{3}$$

The difference between the temperature of the TEG and the air surrounding (ambient temperature) must be taken into account. For all experiments, room temperature is taken to be about 25 ^{0}C. For each drainto source voltage of the

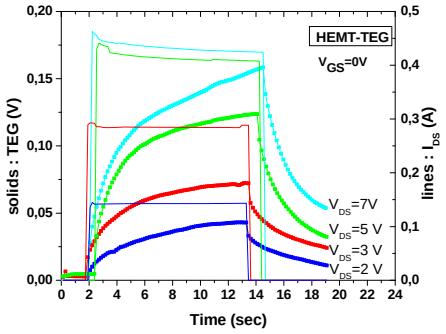


Fig. 9. For V_{GS} = 0V & V_{DS} from 2 to 9 V. TEG's voltage is measured as a function of time (The drain is connected and disconnected manually for each run).

HEMT, the corresponding temperature difference (ΔT) of the TEG is

presented in Table 3.

Table 3. Temperature difference ΔT of the TEG for each drain-source voltage of the HEMT

HEMT V_{DS} (V)	TEG ΔT (^{0}C)
2	42.14
3	59.00
5	73.57
7	77.85

From Table 3, it is clearly shown that for each drain to source voltage, thermo-generated voltage seems to increase exponentially.

Conclusions

The growth of *p*-type (Sb-Te) and *n*-type (Bi-Te) was successfully carried out and the optimum growth parameters were obtained. The stoichiometric ratio for Sb/Te was optimized at 1:3 for *p*-type and the Bi/Te at 1:2 for *n*-type. It is found that the best quality films for *p*-type, S = 150 μV/K, ρ = 15 Ωm and for *n*-type, S = – 52 μV/K, ρ = 8.5 Ωm can be obtained for substrate temperature (T_{sub}) in the range 85 – 90 ^{0}C.

The integration of a TEG on the top surface of the power transistor was designed and manufactured successfully, in order to monitor its temperature indirectly through the thermo-generated voltage. The proof of concept has been experimentally demonstrated for the HEMT-TEG device for the first time. It is concluded that the concept for fabricating the HEMT-TEG device provides a promising procedure as in situ and real time temperature monitoring for power MMICs.

To further improve the efficiency of the TEG sensor we must overcome process constrains and grow TEs at higher T_{sub}

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